CBCS SCHEME

USN | | | | | | | | | | 15EC663

Sixth Semester B.E. Degree Examination, Aug./Sept. 2020
Digital System Design using Verilog

Time: 3 hrs. Max. Marks: 80

Note: ***Answer any FIVE full questions, choosing ONE full question from each module.***

Module-1

1 a. Develop a verilog model that expresses the logical structure of the gate circuit for vat buzzer. Assume that the sensor signals and the switch signal are inputs to the model, and that the buzzer signal is the output from the model. **(04 Marks)**

b. Develop a verilog model for a 7-segment decoder. Include an additional input, blank that overrides the BCD input and causes all segments not to be lit. **(06 Marks)**

c. Develop a data path to perform a complex multiplication of two complex numbers. Whose real and imaginary parts are represented as signed fixed point numbers with 4-pre binary points and 12 post – binary points real and imaginary parts of the product are represented with 8 pre–binary points and 24 post-binary points. Area is the main constraint. **(06 Marks)**

OR

2 a. Explain design methodology followed in IC industry with neat sketch. **(06 Marks)**

b. Develop a test bench model for the traffic light controller. Verify the conditions that, when the enable input is 1, the output is the same as the light input and when the enable input is '0' all light outputs are inactive. **(04 Marks)**

c. Write a verilog code for finite state machine of complex multiple control sequence. **(06 Marks)**

Module-2

3 a. Design 1M × 8 bit composite memory using 512 k × 8 bit memory component. **(04 Marks)**

b. Determine whether there is an error in the ECC word 000111000100 and if so correct it. **(06 Marks)**

c. Develop a verilog model of a dual–port, 4K × 16 bit flow through SSRAM. One port allows data to be written and read. While the other port only allows data to be read. **(06 Marks)**

OR

4 a. Design a 64k × 16 bit composite memory using 16K × 8 bit component. **(06 Marks)**

b. Computer the 12 bit ECC word corresponding to the 8-bit data word 01100001. **(04 Marks)**

c. Design a FIFO to store upto 256 data items of 16 bits each, using a 256 × 16 bit dual-port SSRAM for the data storage. The FIFO should provide status outputs, to indicate, when the FIFO is empty and full. Assume that the FIFO will not be read when it is empty, nor be written to when it is full, and that the write and read ports share a common clock. **(06 Marks)**

Module-3

5 a. Outline with a neat sketch, the internal organization of a CPLD. **(06 Marks)**

b. Design 4-digit decimal counter with seven segment LED display with neat sketch using 74LS390 dual decade counter, four 74LS47 BCD to seven segment decoder, four 7-segment display, plus any additional gates required. **(10 Marks)**

OR

6 a. Outline and explain the internal organization of FPGA. **(08 Marks)**
  b. Explain the concept of differential signaling. How does differential signaling improve noise? **(08 Marks)**

Module-4

7 a. Construct flash ADC and successive approximation ADC with a help of necessary diagram. **(08 Marks)**
  b. Show how a 64-bit data word can be transmitted serially between two ports of a system. Assume that the transmitter and the receiver are both within the same clock domain, and that the signal start is set to 1 on a clock cycle in which data is ready to be transmitted. **(08 Marks)**

OR

8 a. With a net diagram explain R-string DAC and R/2R ladder DAC. **(08 Marks)**
  b. Develop a controller for the keypad matrix and show how to connect the controller to a Gumnut core. Use output port address 4 for the matrix row output register and input address 4 for the matrix column input register. Write the verilog definition for the controller. **(08 Marks)**

Module-5

9 a. Explain the design flow of hardware/software co-design. **(08 Marks)**
  b. Outline the term scan design and boundary scan with neat sketch. **(08 Marks)**

OR

10 a. Demonstrate Built-In Self Test (BIST) techniques. **(08 Marks)**
  b. Illustrate the term design optimization with respect to area, timing and power. **(08 Marks)**

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